CLAIMS

What is claimed is:

Sub B1

1. A method for controlling operation of a multi-pair gigabit transceiver, the multi-pair gigabit transceiver comprising a Physical Layer Control module (PHY Control), a Physical Coding Sublayer module (PCS) and a Digital Signal Processing module (DSP), the method comprising:

receiving at the PHY Control user-defined inputs from the Serial Management module and status signals and diagnostics signals from the DSP and the PCS; and

generating control signals responsive to the user-defined inputs, the status signals and diagnostics signals, from the PHY Control to the DSP and the PCS.

2. The method of Claim 1 wherein the multi-pair gigabit transceiver further comprises an Auto-Negotiation module, the method further comprising:

receiving at the PHY Control a link control signal from the Auto-Negotiation module to start operation of the PCS and the DSP.

3. The method of Claim 1 wherein the multi-pair gigabit transceiver further comprises a Gigabit Medium Independent Interface (GMII) module, the method further comprising:

receiving at the PHY Control a transmit enable signal from the GMII module to start transmission of data packets.

4. The method of Claim 1 further comprises:

receiving a user-defined reset signal at the PHY Control; and

generating a control signal to reset the DSP and the PCS.

5. The method of Claim 1 wherein the control signals include a DSP/PCS reset signal to reset the DSP and the PCS.

6. The method of Claim 1 wherein the DSP comprises a set of echo cancellers and a set of near-end cross-talk (NEXT) cancellers, and wherein the control signals include echo and NEXT control signals to control convergence of the echo cancellers and NEXT cancellers, respectively.

7. The method of Claim 1 wherein the DSP comprises a multi-dimensional decision feedback equalizer (DFE) and wherein the control signals include DFE control signals to control convergence of the multi-dimensional DFE.

8. The method of Claim 1 wherein the DSP comprises a timing recovery (TR) module and wherein the control signals include TR control signals to control convergence of the timing recovery module.

9. A method for controlling convergence of cancellers, a decision feedback equalizer (DFE) and a timing recovery module, the method comprising the operation of:

(a) decoupling the timing recovery module from the cancellers and the DFE while converging the cancellers and the DFE at the same time.

10. The method of claim 9 further comprises the operation of:

(b) converging the cancellers, the DFE and the timing recovery module at the same time after the cancellers and the DFE have converged.

11. The method of claim 9 wherein the operation (a) comprises the operation of ramping up very slowly and linearly the phase output of the timing recovery module.

12. A control module for controlling convergence of cancellers, a decision feedback equalizer (DFE) and a timing recovery module, the control module comprising a state machine for de-coupling the timing recovery module from the

cancellers and the DFE while converging the cancellers and the DFE at the same time.

13. The control module of claim 12 wherein the state machine converges the cancellers, the DFE and the timing recovery module at the same time after converging the cancellers and the DFE at the same time .

14. The control module of claim 12 wherein the state machine de-couples the timing recovery module by ramping up very slowly and linearly the phase output of the timing recovery module.

15. A PHY control module for controlling operation of a multi-pair gigabit transceiver, the multi-pair Ethernet transceiver comprising a Physical Coding Sublayer module (PCS) and a Digital Signal Processing module (DSP), the PHY control module comprising:

a main state machine for receiving user-defined inputs from the Serial Management module and status signals and diagnostics signals from the DSP and the PCS and for generating control signals, responsive to the user-defined inputs, the status signals and diagnostics signals, to the DSP and the PCS.

16. The PHY control module of Claim 15 wherein the multi-pair gigabit transceiver further comprises an Auto-Negotiation module and wherein the main state machine receives a link control signal from the Auto-Negotiation module to start operation of the PCS and the DSP.

17. The PHY control module of Claim 15 wherein the multi-pair gigabit transceiver further comprises a Gigabit Medium Independent Interface (GMII) module and wherein the main state machine receives a transmit enable signal from the GMII module to start transmission of data packets.

18. The PHY control module of Claim 15 wherein the main state machine receives a user-defined reset signal and generates a control signal to reset the DSP and the PCS.

19. The PHY control module of Claim 15 wherein the control signals include a DSP/PCS reset signal to reset the DSP and the PCS.

20. The PHY control module of Claim 15 wherein the DSP comprises a set of echo cancellers and a set of near-end cross-talk (NEXT) cancellers, and wherein the control signals include echo and NEXT control signals to control convergence of the echo cancellers and NEXT cancellers, respectively.

21. The PHY control module of Claim 15 wherein the DSP comprises a multi-dimensional decision feedback equalizer (DFE) and wherein the control signals include DFE control signals to control convergence of the multi-dimensional DFE.

22. The PHY control module of Claim 15 wherein the DSP comprises a timing recovery (TR) module and wherein the control signals include TR control signals to control convergence of the timing recovery module.